# TITLE OF THE INVENTION

IMPEDANCE TRIMMING CIRCUIT

## CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2003-113191, filed April 17, 2003, the entire contents of which are incorporated herein by reference.

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an LSI containing an impedance trimming circuit to execute impedance matching on output impedance, input impedance, terminal resistance, or the like to suppress reflection of signals, thus allowing high-speed serial signals of high quality to be transferred, and in particular, to a trimming circuit for accurate and automatic adjustment.

2. Description of the Related Art

For a high-speed interface such as a USB2.0 (480 Mbps) or an LUDS (several Gbps), it has hitherto been essential to match input impedance, drive impedance, pull-up/pull-down resistance, or the like with a corresponding standard value (for example, ±10%) in order to suppress reflection of the waveform of a transferred signal, thus allowing a high-speed signal of high quality to be transmitted.

However, resistance elements manufactured using an

LSI manufacturing process vary markedly (for example, ±20%). Further, the on resistance of an output transistor depends significantly on a temperature, a power voltage, or a threshold (for example, worst best = double/half). Accordingly, a certain adjustment circuit is required.

A first example of the prior art is Non-patent Document 1 (ESSCIRC2001 "A New Impedance Control Circuit for USB2.0 Transceiver" Koo K.-H. SAMSUNG Electronics (http://www.esscirc.org/esscirc2001/C01_Presentations/5.pdf)).

In Non-patent Document 1, as shown in FIGS. 1 and 2, an operational amplifier adjusts a voltage drop at an external resistor Rext to an internal reference voltage Vref. An output signal from the operational amplifier is supplied to gates of two P channel MOS transistors. An output signal from an output buffer appears as a positive and negative differential outputs at a Data + terminal and a Data - terminal, respectively, on the basis of voltage drops at internal resistors. This circuit has an auxiliary circuit for adjustment in addition to a circuit for data transfer. The auxiliary circuit finds, in a controlled manner, a code that adjusts the potential at a VA terminal to a value Vref.

In this case, output impedance is based on the

internal resistor and MOS resistor. However, in this conventional example, this value is adjusted to 45Ω ± 5Ω. Specifically, a comparator and a control circuit are used to adjust the sizes of the MOS transistors to find a code that results in the smallest error. Then, the sizes of the MOS transistors are increased or reduced, and this code is provided to the output buffer.

However, with this method, the circuit is affected by various variation factors such as a variation in reference voltage, an input offset voltage at the operational amplifier, a variation in the current ratio of a current source composed of the P channel MOS transistors, and a variation in MOS resistance. Thus, actually, it is difficult to accurately adjust the output impedance.

For example, if the current ratio of the current source composed of the P channel MOS transistors varies by about 5%, this mere variation causes the output impedance to reach the limit of the allowable variation range of 45Ω ± 5Ω. Thus, disadvantageously, yield decreases and much labor is required to manage manufacturing steps. Therefore, in reality, it is difficult to accurately adjust the output impedance.

A second example of the prior art is Non-patent Document 2 (ESSCIR2001 "Digitally tuneable on-chip line termination resistor for 2.5 Gbit/s LVDS receiver in

0.25 μm standard CMOS technology" M. Kumric, F. Ebert, R. Rap, K. Welch Alcatel SEL Stuttgart (http://www. esscirc. org/esscirc2001/C01_Presentations/98.pdf)).

In Non-patent Document 2, as shown in FIG. 3, a value for an internal trimming resistor is switched so that the externally provided reference voltage Vref is closest to a divided voltage resulting from an external resistor and the internal trimming resistor. Then, switching codes are used to switch input terminal resistance.

As shown in FIG. 4, the internal trimming resistor is composed of a resistor R0 connected directly between IP and IN and resistors R1 to R8 each connected via a switch turned on and off in a controlled manner using a code.

As shown in FIG. 5, in consideration of the range of a variation in the value for the internal resistor, a value for the resistor R0 is preset at a larger value. The resistors R1 to R8 are sequentially connected together to adjust the value for the internal trimming resistor over a wide range so that it falls within the range of a standard value of 100Ω ± 10Ω.

However, this method requires an external circuit used to generate the reference voltage Vref as well as two external accurate resistors. This advantageously increases costs. Further, this method is used only for an input terminal section. The adjustment of the

output impedance must include the adjustment of the on resistance of the output buffer as shown in the first example of the prior art.

A third example of the prior art is Patent Document 1.

In Patent Document 1 (Jpn. Pat. Appln. KOKAI Publication No. 2001-94048), as shown in FIG. 6, the operational amplifier is used to adjust a current from the current source composed of the P channel MOS transistors so that a voltage drop VZQ at an external resistor PQ is half the voltage at a power source VDDQ. Further, the size of an output driver is adjusted by using a current mirror to allow a current to flow through the output driver so that the resulting voltage drop equals the VZQ.

In this case, a variation in output resistance is affected directly by factors such as the offset voltage at the operational amplifier and a variation in current mirror current. Consequently, accurate adjustment of the current is limited.

It has thus been strongly desirable to provide an impedance trimming circuit which eliminates the adverse effects of variations associated with an LSI manufacturing process to accomplish accurate trimming and which can be constructed using a reduced number of external parts.

## BRIEF SUMMARY OF THE INVENTION

According to an aspect of the present invention, there is provided an impedance trimming circuit comprising a common bias section composed of a first series circuit having a first internal resistor and an external resistor connected in series via a first node and a first operational amplifier having a first input terminal connected to an internal reference voltage, a second input terminal connected to the first node, and an output terminal connected to the first series circuit; and an impedance trimming section composed of a second series circuit having a second internal resistor and an impedance dummy resistor connected in series via a second node, a comparator having a first input terminal connected to the first node and a second input terminal connected to the second node, a code control circuit which uses a clock signal to latch an output signal from the comparator to generate a plurality of switching codes, and a switching circuit which uses the plurality of switching codes to switch a resistance value of the impedance dummy resistor, wherein the first operational amplifier is also connected to the second series circuit, and an output signal from the code control circuit is input to a target impedance trimming circuit.

## BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. 1 is a diagram showing a conventional

impedance trimming circuit;

FIG. 2 is a diagram showing a conventional impedance trimming circuit;

FIG. 3 is a diagram showing a conventional impedance trimming circuit;

FIG. 4 is a diagram showing an example of a conventional trimming resistor;

FIG. 5 is a diagram showing the relationship between codes and the resistance value of the trimming resistance;

FIG. 6 is a diagram showing a conventional impedance trimming circuit;

FIG. 7 is a diagram showing an impedance trimming circuit according to a first embodiment;

FIG. 8 is a graph showing the relationship between codes and output impedance;

FIG. 9 is a graph showing the results of simulation using SPICE;

FIG. 10 is a diagram showing an example of a code control circuit and an impedance dummy resistor;

FIG. 11 is a diagram showing waveforms observed during impedance adjustment;

FIG. 12 is an impedance trimming circuit according to a second embodiment;

FIG. 13 is an impedance trimming circuit according to a third embodiment;

FIG. 14 is a graph showing the relationship

between codes and output impedance according to a fourth embodiment;

FIG. 15 is a diagram showing an impedance trimming circuit according to a fifth embodiment;

FIG. 16 is a graph showing the relationship between codes and the resistance value of an impedance dummy resistor;

FIG. 17 is a graph showing the relationship between the codes and the resistance value of the impedance dummy resistor; and

FIG. 18 is a diagram showing essential elements of an impedance trimming circuit according to an example of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

With reference to the drawings, description will be given of an impedance trimming circuit according to an example of the present invention.

### 1. Outline

First, the impedance trimming circuit according to the example of the present invention has a common bias circuit composed of a reference voltage circuit, an internal resistor R1, an accurate external resistor Rext, and an operational amplifier OP1, and an output impedance trimming circuit composed of another internal resistor Rto, a driver dummy resistor Rdrv, an output impedance dummy resistor Rto_trim, an operational amplifier OP1, a comparator CMP, and a code control

circuit.

The following definitions are assumed: the resistance value of the internal resistor is defined as R1, the resistance value of the accurate external resistor is defined as Rext, the resistance value of the second internal resistor is defined as Rto, the resistance value of the driver dummy resistor is defined as Rdrv, and the resistance value of the output impedance dummy resistor is defined as Rto_trim. Then, the value Rto_trim is switched so as to establish the relationship shown below or the relationship closest to it.

Rext : R1 = (Rdrv + Rto_trim) : Rto

Then, a driver circuit is allowed to reflect this switching information.

The impedance trimming circuit according to the example of the present invention further has an input impedance trimming circuit composed of another internal resistor Rti, an input impedance dummy resistor Rto_trim, an operational amplifier OP2, a comparator CMP, and a code control circuit. A resistance value of this third internal resistor is defined as Rti, and the resistance value of the input impedance dummy resistor is defined as Rti_trim. Then, the value Rti_trim is switched so as to establish the relationship shown below or a relationship closest to it.

Rext : R1 = Rti_trim : Rti

Then, an input impedance circuit is allowed to reflect this switching information

The impedance trimming circuit has only to have at least one of the output impedance trimming circuit and the input impedance trimming circuit. Further, if only the output impedance trimming circuit or input impedance trimming circuit is used or if both impedance trimming circuits are used, a plurality of impedance trimming circuits of each type may be present.

2. First Embodiment

FIG. 7 shows an impedance trimming circuit according to a first embodiment of the present invention.

Reference character Rdrv (symbol Δ) denotes an output driver. A common bias section 11 has the internal resistor R1 and accurate external resistor Rext connected together via a node Vr1, the operational amplifier OP1 to which an internal reference voltage Vref and the voltage at the node Vr1 are inputted, a P channel MOS transistor P1, and an N channel MOS transistor N1. The P channel MOS transistor P1, connected to a power source VDD, is a bias generating circuit used to generate a small-current bias provided to another circuit. This is an accessory circuit.

Operations of this circuit will be described below with reference to FIG. 7.

The operational amplifier OP1 controls a gate

voltage of the N channel MOS transistor (current control element) N1 so that the voltage Vr1 equals the internal reference voltage Vref. The voltage Vr2 is the voltage Vr1 plus a voltage drop at the resistor R1 with a current I1, i.e. $Vr2 = Vr1 + (R1/Rext) \times Vr1$.

A specific example of calculation will be shown below.

The internal reference voltage Vref is assumed to be, for example, 1.2 V ± 5%. The external resistor Rext is assumed to offer an accurate resistance of, for example, 12 KΩ ± 0.1%. The power voltage VDD is assumed to be, for example, 3.3 V ± 10%. The offset voltage at the operational amplifier OP1 is assumed to be, for example, ±10 mV.

A negative feedback circuit composed of the operational amplifier OP1 and the N channel MOS transistor (current control element) N1 operates to make a value for a voltage drop at the external resistor Rext equal to the internal reference voltage Vref. As a result, Vr1 becomes Vref. The accuracy is (1.2 V ± 5%) ± 10 mV, i.e. 1.2 V ± 0.07 V owing to the effects of a variation in internal reference voltage Vref and the offset voltage at the operational amplifier OP1.

The current I1 is equal to Vr1/Rext. The current I1 also varies and is within the range of, for example, 100 μA ± 7 μA. A voltage Vr2 is affected directly by a

variation in a value for the internal resistor R1. If the variation in the value for the internal resistor R1 is, for example, 2.4 KΩ ± 20%, then the voltage Vr2 is given as follows:

$$Vr2 = Vr1+I1\times R1$$
$$= (1.2V\pm 0.07V)+(100\mu A\pm 7\mu A)\times(2.4k\Omega\pm 0.48k\Omega)$$
$$= 1.44V\pm 0.13V$$

Importantly, the voltage Vr2 corresponds to the detection of a ratio containing a difference in resistance value between the internal resistor R1 and the external resistor Rext.

Now, description will be given of an output impedance trimming section 12.

The output impedance trimming section is composed of the comparator CMP to which the voltage Vr1 and a voltage Vto1 are inputted, an operational amplifier OP2 to which the voltage Vr2 and a voltage Vto2 are inputted, a code control circuit 13 that receives an output signal from the comparator CMP, an N channel MOS transistor (current control element) N2, the internal resistor Rto, the output impedance dummy resistor Rto_trim, and the output driver dummy resistor Rdrv.

The operational amplifier OP2 controls a gate voltage of the N channel MOS transistor N2 so that the voltage Vto2 equals the voltage Vr2. In this condition, the voltage Vto1 is divided into Rto and (Rto_trim + Rdrv). However, importantly, the ratio of

Rext to R1 is equal to the ratio of Rto_trim + Rdrv to Rto.

Rext : R1 = (Rto_trim + Rdrv) : Rto

The value for the external resistor Rext is accurate. Thus, even if the value for the internal resistor R1, Rto, Rto_trim, or Rdrv varies, the value Rto_trim + Rdrv can generally be accurately brought into the range of a standard value by manufacturing a circuit so that R1 and Rto have a good relative accuracy.

The code control circuit 13 is composed of, for example, a multistage shift register. An output from the comparator CMP, a result of a comparison of Vr1 with Vto1, is inputted to the multistage shift register that carries out a shifting operation on the basis of a clock signal CLK. A code is obtained from each stage of the shift register to switch among the resistors. To switch among the resistors, it is possible to use, for example, the circuit shown in the second example of the prior art.

Then, as the clock signal CLK is supplied many times, the state is established where the relationship between the potentials Vr1 and Vto1 exhibits the most frequent switching between a positive side and a negative side, i.e. the potentials Vr1 and Vto1 have the closest values that vary between the positive side and the negative side or where the code is stopped and

stabilized. This state corresponds to a code with which the value Rto_trim + Rdrv is closest to the standard.

A specific example of a calculation will be shown below.

If the offset voltage at the operational amplifier is, for example, ±10 mV, then the following equation is given;

$$Vto2 = Vr2 \pm 10\ mV = 1.44\ V \pm 0.13\ V \pm 10\ mV$$
$$= 1.44\ V \pm 0.14\ V$$

A current value Ito is equal to Vto2 / (Rto + Rto_trim + Rdrv).

Because of the current Ito, Vto1 has the following voltage effects:

$$Vto1 = Ito1 \times (Rto\_trim + Rdrv)$$

Consequently, the following equation is established:

$$Vto1 = Vto2/(Rto+Rto\_trim+Rdrv) \times (Rto\_trim+Rdrv)$$
$$= Vto2/(1+Rto/(Rto\_trim+Rdrv))$$

Vto2 is determined by the ratio of Vto2 to resistance.

The comparator CMP selects Rto_trim so that Vr1 is closest to Vrto1. Accordingly, on this occasion, if the offset voltage at the comparator CMP is defined as Voffcmp (±20 mV), then the following equation is given:

$$Vto1 = Vr1 \pm Voffcmp$$

Specifically, the right

side = 1.2 V ± 0.07 V ± 0.02 V = 1.2 V ± 0.09 V.

If the right side equals the left side Vtol, then the following equation is established:

1.2V±0.09V = (1.44V±0.14V)/(1+Rto/(Rto_trim+Rdrv)

Here, it is assumed that the output impedance trimming circuit composed of Rto and (Rto_trim + Rdrv) offers resistance that is, for example, six times as large as that of an actual output buffer circuit in order to reduce current consumption. Accordingly, if an actual driver output impedance is to be 45Ω, then Rto_trim + Rdrv is 270Ω.

Rto is 54Ω on the basis of the relationship Rext:R1 = (Rto_trim + Rdrv):Rto, i.e. 12 KΩ:2.4 K = 270Ω:54Ω.

Further, it is assumed that Rto_rim + Rdrv = 270Ω, Rto_trim = 240Ω, and Rdrv = 30Ω.

Importantly, the resistors R1 and Rto are formed within the same integrated circuit and can thus be manufactured so as to have a good relative accuracy. Further, the resistor Rto_trim can also be manufactured so as to have a good relative accuracy. However, since the resistor Rdrv is composed of, for example, a MOS transistor, its variation contains a variation associated with the manufacture of the transistor.

This is substituted into the previous equation.

1.2V±0.09V=(1.44V±0.14V)/(1+(Rto/(Rto_trim+Rdrv))

Then, the following equation is established:

Rto/(Rto_trim + Rdrv)

= ((1.44V ± 0.14V)/(1.2V ± 0.09V))-1

Accordingly, the adjusted resistance value Rto_trim is written on the left side, the following equation is given:

Rto_trim=(Rto/((1.44V±0.14V)/(1.2V±0.09V))-1)-Rdrv

Specific values are substituted into the above equations.

If the following assumptions are made:

Rdrv = 30Ω ± 20Ω,

Rto = 54Ω ± 10.8Ω

then the following equation is given:

Rto_trim = ((54Ω ± 10.8Ω) / ((1.44V ± 0.14V) / (1.2V ± 0.09V)-1))-(30Ω ± 20Ω)

If a center condition is used for all cases, then the following calculation can be executed:

Rto_trim(center) = (54Ω/((1.44V/1.2V)-1))-30Ω

= 240Ω

That is, if Rto_trim is adjusted to be closest to 240Ω, the final value is determined to be 240Ω. If the value for the resistor Rdrv connected in series with the resistor Rto_trim is added to this final value, then 30Ω + 240Ω = 270Ω. Thus, the resistance is accurately adjusted to a value that is six times as large as the target one, i.e. 45Ω.

Variations in various factors can be determined using the above calculation. However, this requires

various calculations and their description is thus omitted. An important point is that a wide range of variation is assumed so that the value for the output impedance dummy resistor Rto_trim can be adjusted over a wide range.

FIG. 8 shows an example of an adjustment range for the trimming circuit.

Actually, under the same conditions as those for the driver circuit, too large a current may flow. Thus, to limit the current, the value for the output impedance dummy resistor Rto_trim is designed to be about six times as large as the target value. Table 1, shown below, shows this value in terms of the impedance of the output driver.

Table 1

| Rtrm | 53.33 | *0.8 | *1.2 | *0.9 | *1.1 |
|---|---|---|---|---|---|
| Rsw | 5 | 3 | 8 | 3 | 8 |
| Code | Typ | (-20%) | (+20%) | (-10%) | (+10%) |
| 0 | 58.33 | 45.67 | 72.00 | 51.00 | 66.67 |
| 1 | 53.70 | 41.96 | 66.43 | 46.83 | 61.57 |
| 2 | 40.80 | 38.84 | 61.76 | 43.32 | 57.28 |
| 3 | 46.48 | 36.19 | 57.78 | 40.33 | 53.63 |
| 4 | 43.62 | 33.90 | 54.34 | 37.76 | 50.48 |
| 5 | 41.13 | 31.90 | 51.35 | 35.53 | 47.74 |
| 6 | 38.94 | 30.15 | 48.73 | 33.55 | 45.33 |
| 7 | 37.00 | 28.60 | 46.40 | 31.80 | 43.20 |

This table shows how the output impedance of the actual driver varies when the code control circuit 13

is switched among eight states obtained by constructing the code control circuit 13 using a 7-stage shift register.

This graph contains the range of a variation and is based on the assumptions that Rto_trim is 20% and that a switch required for switching operations offers resistance 5Ω + 3Ω / -2Ω.

For calculations, it is assumed that the resistance value of each switch = 5Ω, R1, ... R7 = 560Ω, and the driver resistance Rdrv = 5Ω.

In consideration of a variation in the value for the internal resistor, Rto_trim + Rdrv is set so as to be arbitrarily switched within a certain range around a target value (in this case, 45Ω) using codes.

For example, for the driver circuit, Rto + Rdrv is set to be 58.33Ω at maximum and 37Ω at minimum. Cases indicated by *0.8 and *1.2 are examples of calculations that take various variations or dependencies into consideration. Under a standard condition, the optimum value of 45Ω lines between codes 3 and 4. However, under the best condition indicated by *0.8, the optimum value is found between codes 0 and 1. Under the worst condition indicated by *1.2, the optimum value is found between codes 6 and 7.

It is evident that even if the standard value is set at 45Ω ± 5Ω, the value can be adjusted even with a variation of ±20% in the value for the internal

resistor.

Consequently, Vt1 ≒ Vto2, Ito, and others are controlled so that Vr1 equals Vto1. Therefore, the values including Vref are only intermediate variables for a control system the final result of which is an accurate resistance ratio. It is thus evident that direct effects have been eliminated.

Furthermore, importantly, although not shown in detail, the present circuit is very insensitive to Vref, the offset voltage at the operational amplifier OP1, a variation in current, and the like. The resistance ratio of R1 to Rto must be accurate, but a relative accuracy of ±0.5% or less can be easily accomplished by arranging these resistors so as to occupy a certain area or larger in the LSI and to lie close to each other.

FIG. 9 shows the results of circuit simulation using SPICE except for the impedance trimming circuit Rtrim.

In this figure, the axis of ordinate indicates Vto1 to Vr1, an input to the comparator CMP, while the axis of abscissa indicates the elapsed time from 0 to 10 μs. This figure shows the results of simulation obtained by linearly varying the value Rtrim. Even if the ranges of variations described above are combined together 100 times using a Monte Carlo method, all lines other than the lower two cross a 0-V line. This

indicates the possibility of adjustment.

FIG. 10 shows an example of the code control circuit and impedance trimming circuit.

In this case, the comparator CMP that outputs 1 when Vto1 > Vr1 uses the clock signal CLK to latch information indicative of a decrease in resistance (the code is increased to turn the switch for Rtrim on) and to perform a sequential shifting operation.

In this case, provided that all resistors with switches which constitute the impedance trimming circuit have the same configuration, all that is important is which stage of the multistage shift register is outputting 1. Accordingly, no problems result from the sequential shifting operation. In an initial state, even if all shift registers have a value of zero, the optimum code can be generated by providing the clock signal CLK many times.

Normally, the optimum value is determined by sequentially and repeatedly shifting the code between Vto1 $\geq$ Vr1 and Vto1 $\leq$ Vr1. However, even if all resistors are connected together in parallel, the code is determined if Vto1 $\geq$ Vr1. Even if all shift registers exhibit a value of zero, i.e. they indicate the largest resistance, the code can be determined if Vto1 $\leq$ Vr1.

The operational waveform diagram in FIG. 11 indicates this adjustment.

This figure shows how the state changes.

3. Second Embodiment

FIG. 12 shows an impedance trimming circuit according to a second embodiment of the present invention.

This embodiment relates to an input impedance trimming circuit 14. Compared to the above output impedance trimming circuit, this circuit does not require any driver dummy resistors or drivers but simply trims resistance and uses the code obtained to adjust the input impedance.

Operations of this circuit are the same as those in the first embodiment. Their description is thus omitted.

4. Third Embodiment

FIG. 13 shows an impedance trimming circuit according to a third embodiment of the present invention.

This embodiment relates to an I/O impedance trimming circuit. This circuit has the output impedance trimming section 12 and the input impedance trimming section 14. In this case, a single common bias section 11 can be shared by the output impedance trimming section 12 and the input impedance trimming section 14.

Operations of this circuit are the same as those in the first embodiment. Their description is thus

omitted.

5. Fourth Embodiment

FIG. 14 shows an impedance trimming circuit according to a fourth embodiment of the present invention.

This embodiment relates to a resistance adjustment circuit.

With the method shown in the second example of the prior art, the impedance is adjusted by connecting the resistor R0 in parallel with the resistors R1 to R8 having the same resistance value as the resistor R0. However, this method is disadvantageous in that the number of code increases with the allowable variation range and that it is necessary to switch the resistance over a wide range from smaller to larger resistance.

In this embodiment, the relationship between the code and the resistance value is represented by an S-shaped curve or a polygonal line. Accordingly, even with a wide range of variation, the impedance can be adjusted using a small number of codes.

Specifically, for example, in the second example of the prior art, the value for the resistor R0 is set at 55Ω. The value for the resistors R1 and R2 is set at 67Ω. The value for the resistors R3, R4, and R5 is set at 100Ω. The value for the resistor R6 is set at 42Ω. The value for the resistor R7 is set at 33Ω. In this manner, the different resistance values are used

for the respective resistors so that the relationship between the code and the resistance value is represented by an S-shaped curve or a polygonal line.

In this regard, a decode circuit may be provided which serves to change the resistance values used for adjustment. Rather than using simple shift registers for switch control, this decode circuit detects the number of level 1 on the basis of an output from each stage of the multistage shift register, to select resistors to be connected in parallel on the basis of this number.

6. Fifth Embodiment

FIG. 15 shows an impedance trimming circuit according to a fifth embodiment of the present invention.

This embodiment relates to a resistance adjustment circuit and is an applied example of the resistance adjustment shown in the first embodiment.

The LSI has the following parasitic resistances: lead frame resistance, bonding wire resistance, intra-pellet wiring resistance, and the like, which are parasitic on a package. Thus, from the outside of the package, the impedance of the LSI appears like a series connection of all these resistances. In this embodiment, all these parasitic resistances are estimated before the value for the impedance dummy resistor Rtrim is adjusted. Then, the impedance is adjusted to

exhibit a desired value with all parasitic resistances present.

For example, if wiring resistance Rmetal is 0.5Ω, bonding wire resistance Rbdg is 0.3Ω, and lead frame resistance Rfrm is 0.2Ω, then the resistance of the whole current path from power pin to output pin of the buffer is $2 \times (0.5\Omega + 0.3\Omega + 0.2\Omega) = 2\Omega$.

In such a case, the impedance dummy resistance Rtrim may be adjusted to a value smaller than the desired resistance value, 45Ω, by about 2Ω, i.e. 43Ω. However, with the present circuit, it is cumbersome to switch the value for the impedance dummy resistor Rtrim around this value, 43Ω.

In this embodiment, the adjustment range of the value for the impedance dummy resistor Rtrim can be shifted by switching the value for the resistor R1.

If Rext:R1 = Rtrim:Rt and Rtrim is to be changed from 45Ω to 43Ω for adjustment, the value R1 may be increased by a value of 45/43. In this case, to allow the value R1 to be switched with all expected parasitic resistances taken into account, an LSI pattern may be provided before the value R1 is increased or reduced. A switching operation may be performed by using an analog switch, switching the metal layer using a master slice, or using other methods.

FIGS. 16 and 17 show an example of a variation in resistance with respect to the code observed if the

value for the impedance dummy resistor Rtrim is switched with the parasitic resistances taken into account.

As shown in these figures, if the parasitic resistances are small, the value for the impedance dummy resistor Rtrim can be switched around a larger value, e.g. 43Ω. On the other hand, if the parasitic resistances are large, the value for the impedance dummy resistor Rtrim can be switched around a smaller value, e.g. 40Ω.

Even with a different package, the impedance can be kept constant according to this embodiment.

7. Sixth Embodiment

Now, description will be given of an impedance trimming circuit according to a sixth embodiment of the present invention.

This embodiment is a variation of the above described fifth embodiment. Specifically, in FIG. 15, the value for the accurate resistor Rext need not necessarily be singular. For example, if the accurate resistor Rext has a resistance value of 12 kΩ, the value for the resistor R1 is set at 2.4 kΩ. On the other hand, if the accurate resistor Rext has a resistance value of 13 kΩ, the value for the resistor R1, 2.4 kΩ, may be increased by (13/12) × 2.4 kΩ up to 2.6 kΩ.

Operations of this circuit are omitted, but the

relationship Rext:R1 = Rtrim:Rt is maintained.

Thus, the impedance can be kept constant even with a change in the value for the accurate resistor Rext.

8. Seventh Embodiment

Now, description will be given of an impedance trimming circuit according to a seventh embodiment of the present invention.

This embodiment is a combination of the above described fifth and sixth embodiments. When the fifth and sixth embodiments are thus combined together, the resistance value of the resistor R1 can be switched to correct the resistance value of the accurate resistor Rext and the values for various resistances parasitic on the package. That is, the impedance can be kept constant even with a change in the value for the accurate resistor Rext or in the type of the package.

9. Eighth Embodiment

Now, description will be given of an impedance trimming circuit according to an eighth embodiment of the present invention.

This embodiment relates to measures taken if the internal reference voltage Vref deviates from the desired value in the above described fifth embodiment. For example, it is assumed that the target value for the internal reference value is 1.2 V and that the value for the accurate resistor Rext is 12 kΩ. In this case, a current flowing through the accurate resistor

Rext is Vref/Rext = 100 μA.

Here, the internal reference voltage Vref may deviate from 1.2 V owing to a change in manufacturing process or the like. If the internal power voltage Vref becomes 1.25 V, then a current of 125 μA flows through the accurate resistor Rext. The voltage Vr2 also increases with a voltage drop at the resistor R1.

In such a case, the resistor R1 is divided into two parts, and the midpoint between these parts is defined as Vr1 and connected to a negative input terminal of the operational amplifier OP1. Then, a potential difference of 1.25 V - 1.2 V = 0.05 is absorbed by one (the lower part of R1) of the two parts which is connected to the accurate resistor Rext. Further, the other part (the upper part of R1) connected to an output terminal of the operational amplifier OP1 has a resistance value that meets the relationship Rext:(lower part of R1 + upper part of R1) = Rtrim:Rt.

Thus, according to the present embodiment, even with a variation in internal reference voltage Vref, the operational current can be kept constant. Therefore, the value Rtrim can be accurately adjusted.

10. Conclusion

As described in the first to eighth embodiments, the following effects are produced by the impedance trimming circuit according to the example of the

present invention:

• The circuit can be manufactured using a normal CMOS LSI manufacturing process.

• Only one external resistor is required. This is advantageous in terms of costs.

• The impedance can be kept constant even with a change in the value for the external accurate resistance.

• The impedance can be kept constant even with a change in the layout of the LSI or in parasitic resistance.

• The number of adjustment codes can be easily increased to easily accomplish accurate adjustments.

• The adjustment of the output impedance is also executed on the driver and is thus very accurate.

• The yield can be easily increased in spite of a wider range of variation.

• The circuit can be divided into a number of elements. Accordingly, the elements can be easily shared, and the area of the circuit can be reduced.

FIG. 18 shows the essential elements of the present invention which are used to accomplish these effects. The concept of the present invention is that for the resistance values of the resistance elements, the value Rtrim is set so as to establish a relationship closest to Rext:R1 = Rtrim:Rt.

Further, it should be appreciated that within the

scope of this concept, the following variations are possible.

• The P channel MOS transistor (current driver) is connected to the power terminal VDD in order to increase an output current from a power amplifier.

• Likewise, a source follower of the N channel MOS transistor is connected to the power terminal VDD.

• The resistor R1 is formed inside the LSI so that the resistance value of the resistor R1 can be varied in accordance with the resistance value of the external resistor Rext.

• The code control circuit is composed of a latch and a coder instead of the multistage shift register.

• The number of states of a code signal is increased or reduced on the basis of the relationship between the adjustable variation range and adjustment accuracy.

• Unit resistors of the same shape are arranged close to each other within the LSI in order to improve the relative accuracy for the resistors R1 and Rt.

• The relationship between the reference voltage Vref and the power voltage VDD is kept constant, and the relationship between the power voltage VDD and ground voltage VGNBD of the whole circuit is reversed.

• The value for the resistor Rt is adjusted rather than adjusting the value for the resistor R1 in accordance with the value for the external resistor

Rext and the parasitic resistance.

• A fixed ratio is maintained between the resistor Rtrim for a feedback system and an actual target impedance trimming circuit (an output driver section and an input resistance section).

As described above, according to the impedance trimming circuit according to the example of the present invention, an accurate trimming operation can be performed by eliminating the adverse effects of variations associated with the LSI manufacturing process. Further, the circuit can be constructed using a reduced number of external parts, thus reducing manufacturing costs.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.